

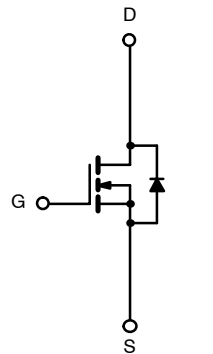
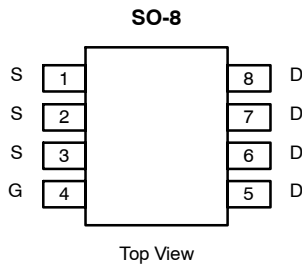


## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.0135 @ $V_{GS} = 10$ V	10
	0.020 @ $V_{GS} = 4.5$ V	8

### FEATURES

- TrenchFET® Power MOSFET



Ordering Information: Si4410DY-REVA  
 Si4410DY-T1-REVA (with Tape and Reel)  
 Si4410DY-REVA-E3 (Lead free)  
 Si4410DY-T1-A-E3 (Lead free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	10
		$T_A = 70^\circ\text{C}$	8
Pulsed Drain Current	$I_{DM}$	50	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.3	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 70^\circ\text{C}$	1.6
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	50	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	22	

Notes  
 a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

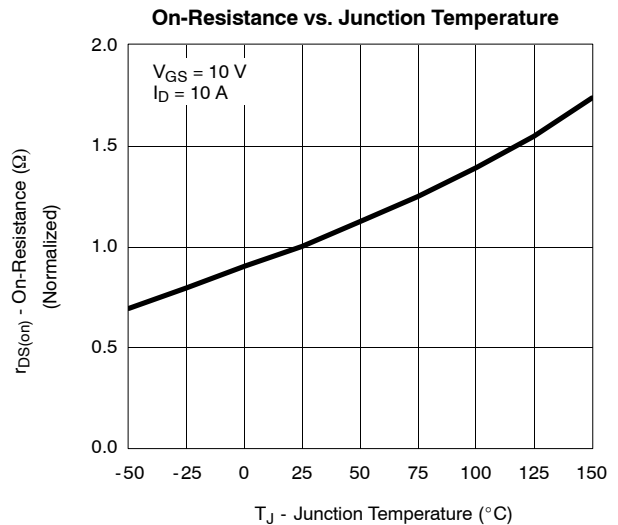
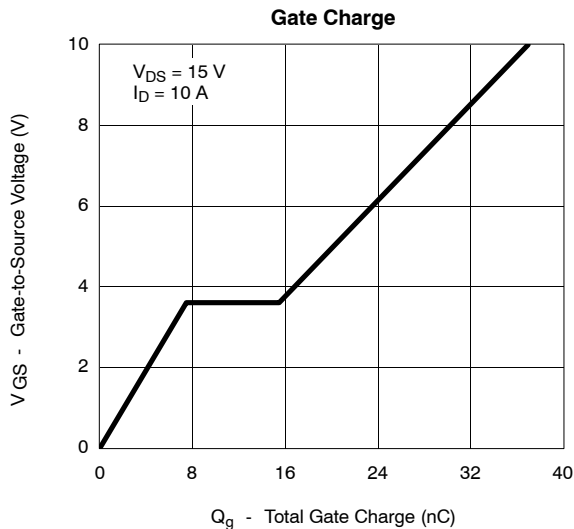
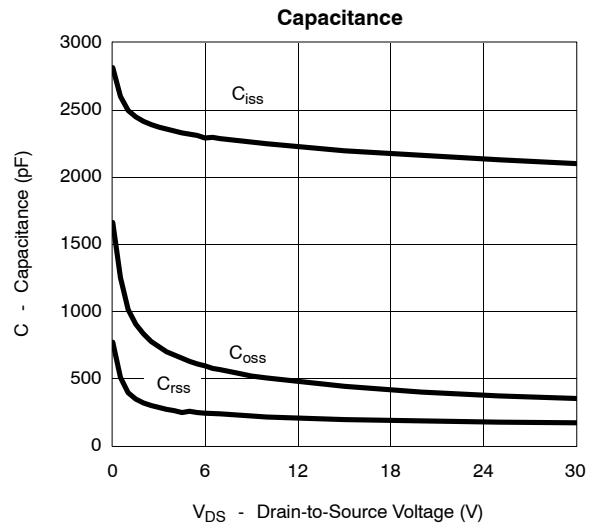
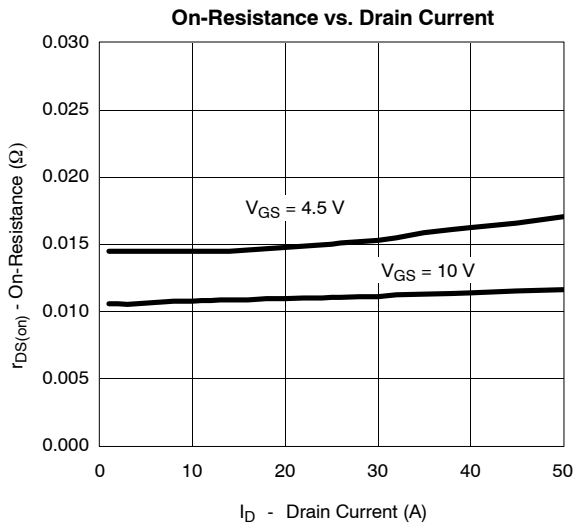
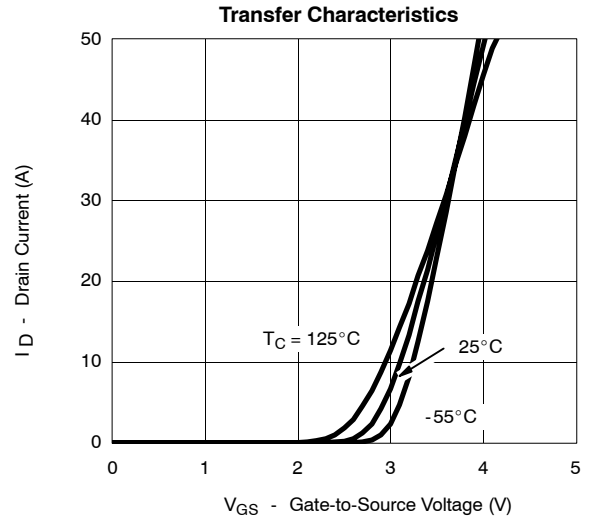
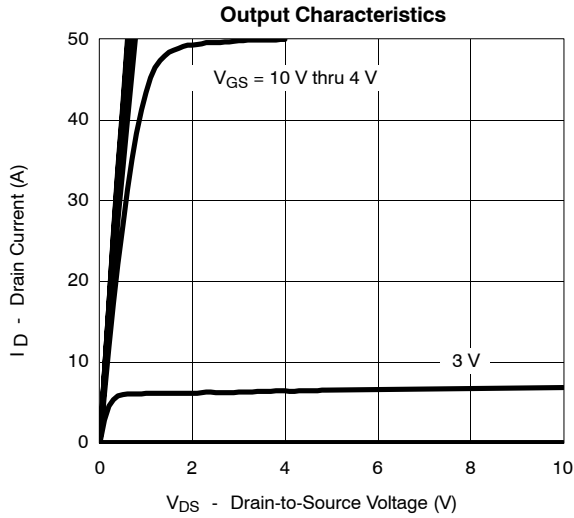
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			25	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.011	0.0135	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		0.015	0.020	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		38		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.3 A, V <sub>GS</sub> = 0 V		0.7	1.1	V
<b>Dynamic<sup>b</sup></b>						
Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 10 A		20	34	nC
Total Gate Charge	Q <sub>gt</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		37	60	
Gate-Source Charge	Q <sub>gs</sub>			7		
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		7.0		
Gate Resistance	R <sub>g</sub>		0.5	1.5	2.6	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		19	30	ns
Rise Time	t <sub>r</sub>			9	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			70	100	
Fall Time	t <sub>f</sub>			20	80	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.3 A, di/dt = 100 A/μs		40	80	

## Notes

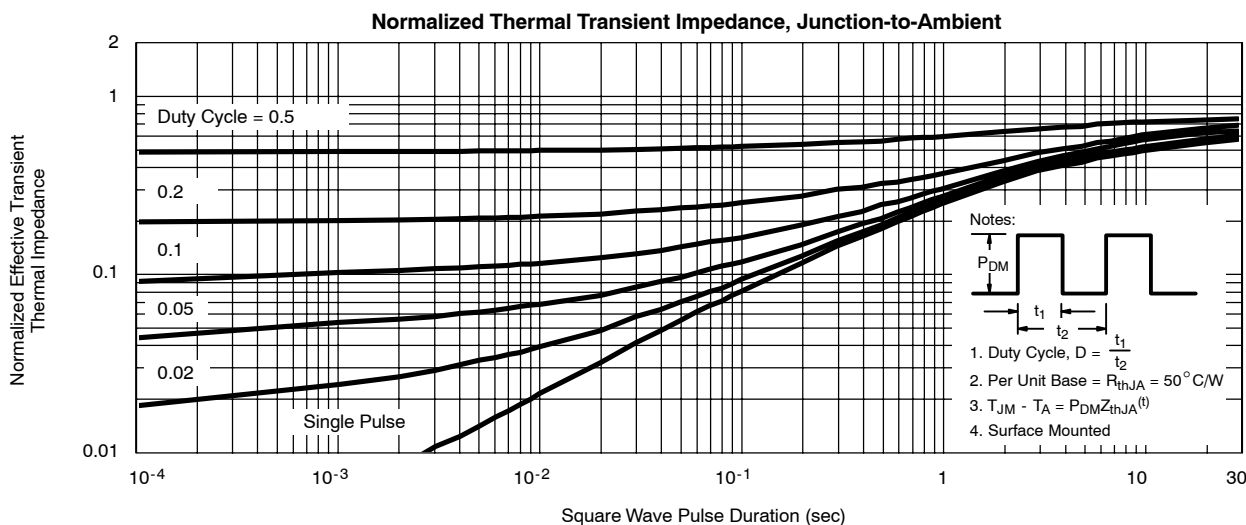
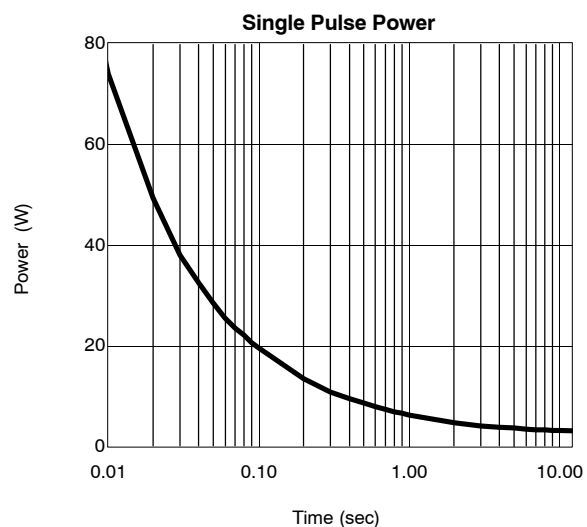
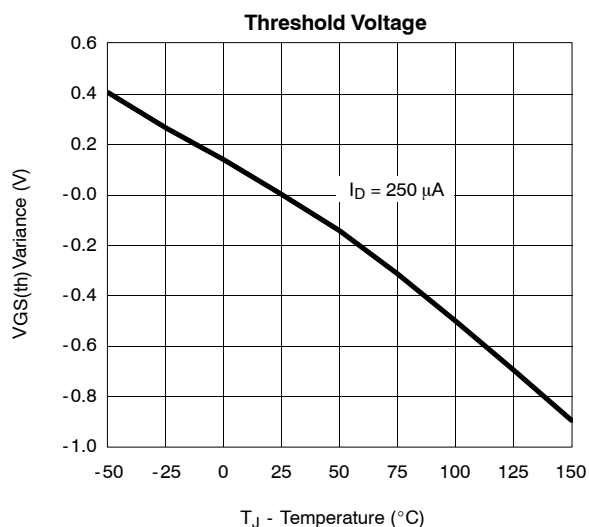
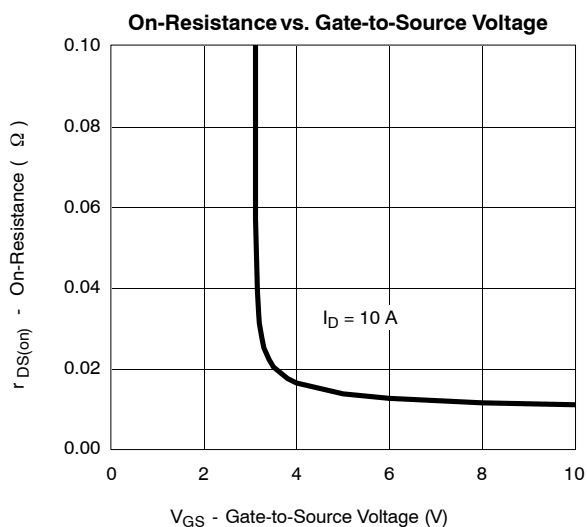
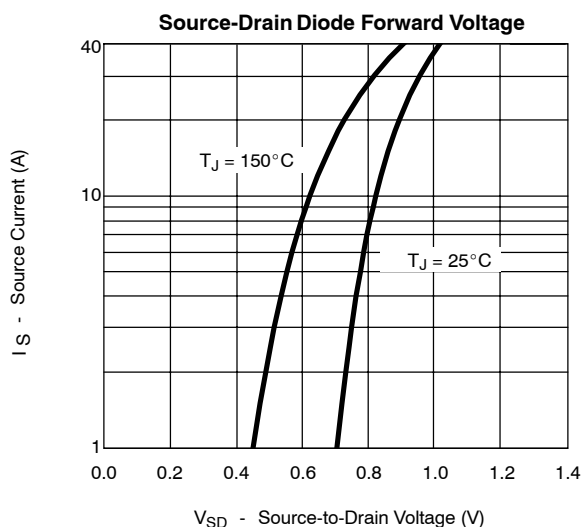
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing. Values shown are for product revision A.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



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